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## ABSTRACT

We present the current state of the art in micro-transfer printing for heterogeneously integrated silicon photonic integrated circuits. The versatility of the technology is highlighted, as is the way ahead to make this technology a key enabler for next-generation photonic systems-on-chip.

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## I. INTRODUCTION

Silicon photonics (SiPh) (comprising both Si and SiN-based waveguide circuits) is becoming an established platform for the realization of complex photonic integrated circuits (PICs),<sup>1–3</sup> especially at telecommunication wavelengths<sup>4–8</sup> but rapidly expanding toward the visible/UV<sup>9,10</sup> and short-wave infrared.<sup>11–14</sup> However, the platform lacks a number of optical functions that cannot be natively integrated: gain elements, typically realized in III–V semiconductors; detectors beyond 1600 nm wavelength (III–V semiconductors); electro-optic modulators [LiNbO<sub>3</sub>, BaTiO<sub>3</sub> (BTO), and PbZr<sub>x</sub>Ti<sub>1-x</sub>O<sub>3</sub> (PZT)]; electro-absorption modulators outside the C+L-band; optical isolators and circulators based on magneto-optic materials; single-photon sources and detectors for quantum applications; etc. Heterogeneous integration will be key to enabling these functionalities on a SiPh wafer. For III–V device integration, sev-

eral approaches are being pursued to enable this: the pick-and-place of packaged lasers, the flip-chip integration of bare III–V dies,<sup>15–17</sup> die-to-wafer bonding<sup>18–20</sup> processes, and the hetero-epitaxial growth of III–V semiconductors on Si.<sup>21–24</sup> Each of these approaches has its advantages and drawbacks, as well as a different level of technology readiness and availability. As more (and different) types of devices need to be integrated, a scalable and versatile heterogeneous integration approach is required. Micro-transfer printing ( $\mu$ TP) is a technology that ticks many of the boxes: de-coupling of the processing of the SiPh and the non-native components, efficient evanescent optical interfacing between printed components and the SiPh, possibility to pre-test/inspect the components on the source wafer (known good die), efficient utilization of the source material as the devices can be integrated in dense arrays on the source wafer 70  $\mu$ m device pitch is a typical value,<sup>25</sup> compared to  $\sim$ 300  $\mu$ m for flip-chip integrated devices,<sup>26</sup> high-throughput integra-

tion of the components on the SiPh wafers after the back-end-of-line is completed, high alignment accuracy ( $\pm 0.5 \mu\text{m } 3\sigma$ ),<sup>27</sup> etc. It is also a very versatile technology as it enables the (co-)integration of devices made in different material systems (III–V semiconductors, Si, electro-optic materials, magneto-optic materials, etc.), as will be made clear in the next section.

$\mu$ TP relies on the fabrication of dense device arrays on a source wafer, followed by their release and transfer in a parallel fashion to a SiPh target wafer using a polydimethylsiloxane (PDMS) stamp. By patterning the PDMS stamp, the dense device array on a (small) source wafer can be scaled out to a sparse device array on a (large) target wafer, as illustrated in Fig. 1. The pick-up and printing processes depend on the visco-elastic properties of the PDMS. After lamination of the stamp to the source wafer, the stamp is pulled back quickly, introducing a strong adhesion between the coupon and the stamp, thereby breaking the tethers. The printing operation relies on a slow retraction of the stamp, thereby lowering the adhesion between the stamp and the coupon. A full printing cycle

takes between 30 and 45 s, while over 30 000 print cycles can be done with a single PDMS stamp.<sup>28</sup>

$\mu$ TP is considered a next-generation heterogeneous integration technology, with several advantages compared to established integration approaches, such as the integration of laser-micro-package devices through active alignment, passive alignment flip-chip integration, and die-to-wafer bonding. This is summarized in Table I. While it has several technical advantages, the technology-readiness-level for its use in heterogeneous Si PICs is still modest. This will be discussed further in Sec. III.

The integration of non-native devices on a complex SiPh platform typically requires defining a recess in the back-end stack to reach the Si or SiN device layer in the case of evanescent coupling or the Si substrate in the case of butt-coupling, followed by the application of an adhesive bonding layer (divinyl-siloxane-bis-benzocyclobutene (DVS-BCB) or Intervia) in the recess, typically through a spray coating process. Next, the non-native devices are printed with high alignment accuracy, followed by the curing of the DVS-BCB and a final metallization to connect the devices to the SiPh back-end if necessary. This is illustrated in Fig. 2 for III–V opto-electronic components, such as lasers, amplifiers, or modulators. A similar approach can be followed for, e.g., electro-optic and magneto-optic materials. The dense co-integration of different devices, implemented in different material systems, can be realized this way. Therefore,  $\mu$ TP technology shines when the heterogeneous integration complexity is high. It can also be considered the “Swiss army knife” of heterogeneous integration due to its versatility, enabling fast innovation. In the short term, we see business cases in the heterogeneous integration of LiNbO<sub>3</sub> on SiPh wafers for 100 GBaud + modulation as well as the integration of semiconductor optical amplifiers (SOAs) to compensate losses in complex PICs. Pilot lines are being setup to offer this technology, both at the prototyping level (e.g., in imec) and in high-volume production (i.e., in X-FAB).

II. MICRO-TRANSFER PRINTING DEMONSTRATIONS

$\mu$ TP requires careful consideration of the release layers and the release processes, depending on the material systems used. An overview of the material systems, their release layer, and release chemistry (wet/vapor etching) is illustrated in Table II. Thin-film materials such as LiNbO<sub>3</sub>, PZT, BTO, 2D materials, Ce:YIG, colloidal quantum dot (QD) films, superconducting NbTiN, Ti:sapphire, etc. can be deposited or bonded either on a Si wafer, oxidized Si wafer, or SOI wafer, allowing the use of SiO<sub>2</sub> or Si as the release layer.

In the following subsections, a mini-review is carried out.

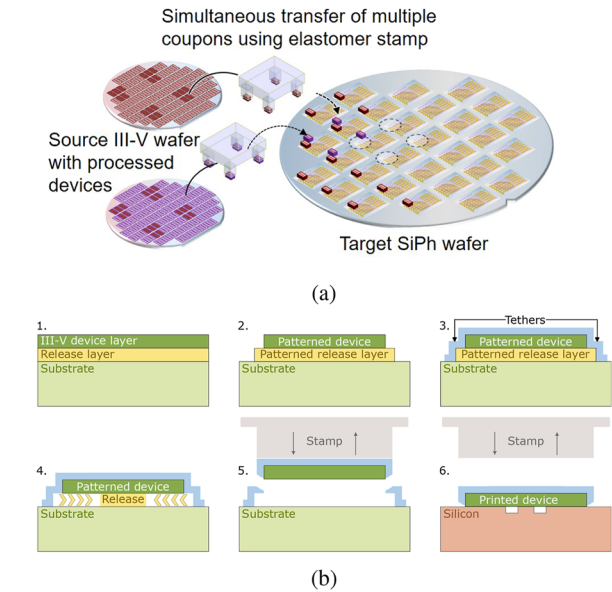


FIG. 1. Concept of  $\mu$ TP. (a) Schematic of  $\mu$ TP-based integration on 200 or 300 mm SiPh wafers in a parallel manner, and (b) prefabrication of III–V devices on their native substrate and the  $\mu$ TP integration sequence.

TABLE I. Comparison of different III–V-on-Si wafer-level heterogeneous integration approaches.

Technology	Integration density	CMOS compatibility	Efficiency of III–V material use	Alignment accuracy	Throughput	Cost	Maturity
Flip-chip	Low	Back-end compatible	Medium	Medium	Low	High	Mature
Bonding	Medium	Back-end compatible	Medium	High	High	Medium	Mature
Epitaxial growth	High	Potentially front-end compatible	Very high	High	High	Medium	R&D
$\mu$ TP	High	Back-end compatible	High	Medium	High	Low	R&D

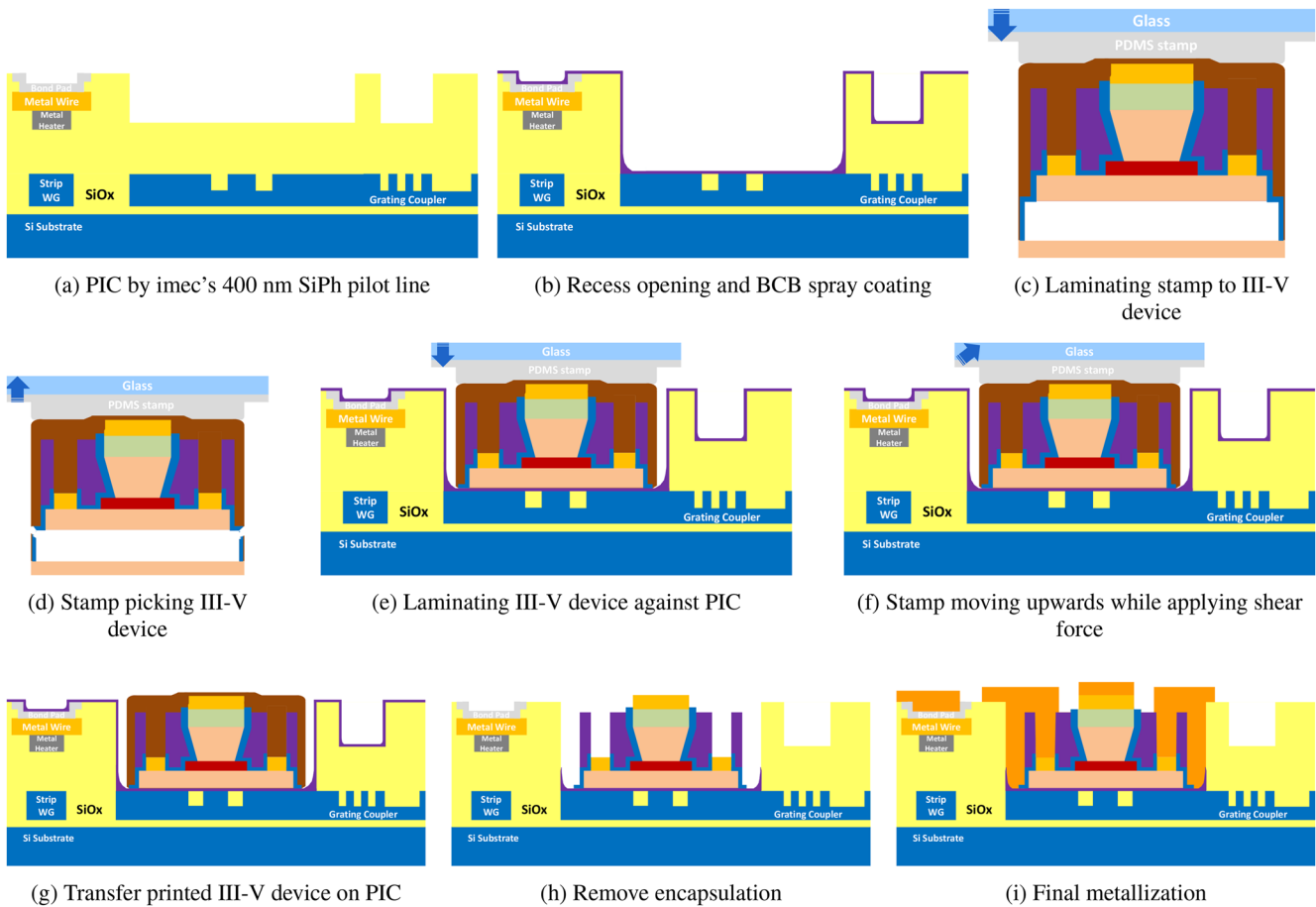


FIG. 2. Process flow of PIC preparation, transfer printing, and post-processing (image from Ref. 29).

TABLE II. Sacrificial layers and etch chemistries used in different material systems.<sup>30,31</sup>

Material system	Release layer	Etchant
InP	InGaAs	FeCl <sub>3</sub> <sup>32</sup>
InP	AlInAs	FeCl <sub>3</sub> <sup>32</sup>
GaAs	Al <sub>x</sub> Ga <sub>1-x</sub> As ( $x > 0.5$ )	HF, <sup>33</sup> HCl <sup>34</sup>
GaAs	InAlP, InGaP	HCl <sup>14,35</sup>
GaP	AlGaP	HF <sup>36</sup>
SOI	SiO <sub>2</sub>	HF (liquid or vapor) <sup>37</sup>
SiO <sub>2</sub>	Si	TMAH, <sup>27,38</sup> KOH <sup>27</sup>
LiNbO <sub>3</sub>	SiO <sub>2</sub>	BOE, HF <sup>39,40</sup>
LiNbO <sub>3</sub>	Si	Xe <sub>2</sub> F <sub>4</sub> <sup>41</sup>
AlGaIn	Si	TMAH, KOH, <sup>42</sup>
		SF <sub>6</sub> -C <sub>4</sub> F <sub>8</sub> (ICP) <sup>43</sup>
Ce:YIG	SiO <sub>2</sub>	Dilute HF <sup>44</sup>
Diamond <sup>45</sup>	No release layer	...

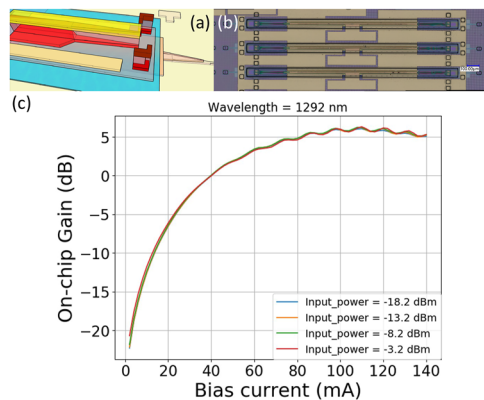
A. GaAs

Gallium Arsenide (GaAs)-based material systems offer superior electrical and optical properties that can be tuned by adjusting the composition of the involved elements and/or the epitaxial structures. They are suitable for the development of high-performance lasers, photodiodes, and nonlinear components for a wide range of applications. The 6 in. GaAs wafer technology is well developed in foundries.<sup>46</sup> In this section, various transfer-printed devices operating at different wavelengths ranging from the near-infrared to the O-band are introduced. These demonstrations include SOAs, distributed-feedback (DFB) lasers, Fabry-Pérot (F-P) lasers, vertical-cavity surface-emitting lasers (VCSELs), photodiodes, and nanocavity lasers. In addition, AlGaAs microdisks operating in the C-band are introduced.

1. Evanescently coupled SOAs

SOAs are essential components in PICs, especially in integrated optical transceivers. They can be deployed as booster amplifiers



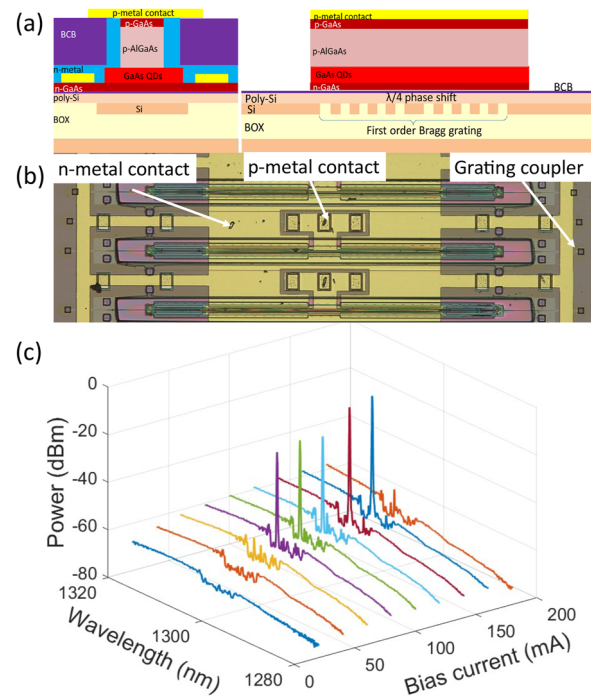


**FIG. 3.** O-band integrated SOAs based on GaAs QD gain coupons. (a) Schematic layout of the alignment-tolerant III-V/Si taper structure. (b) Microscope image of an array of resulting devices. (c) Measured on-chip gain as a function of bias current for different waveguide-coupled input power at 1292 nm.

after the transmitter or as pre-amplifiers before receivers. They also have the potential to work as switches<sup>47</sup> and wavelength converters.<sup>48</sup> Recently, O-band InAs/GaAs QD-on-Si integrated SOAs were demonstrated using  $\mu$ TP. The GaAs epitaxial structure used in this work consists of 12 layers of GaAs/InAs QD and a 500 nm thick AlGaAs sacrificial layer for the undercutting of fabricated SOA device coupons. The SiPh target substrate is fabricated using imec's iSiPP50G technology, consisting of a 220 nm thick crystalline Si device layer, a 160 nm thick poly-Si overlay layer, and a 5  $\mu$ m thick multi-layer back-end stack. An alignment-tolerant III-V/Si taper structure was designed to accommodate the alignment accuracy of the  $\mu$ TP system, as shown in Fig. 3(a). The SOAs were demonstrated by  $\mu$ TP a pre-fabricated 1.66 mm long GaAs QD SOA coupon onto a poly-Si/crystalline Si hybrid rib waveguide with a thin BCB adhesive layer in between. The pre-fabricated device consists of a 980  $\mu$ m long straight GaAs rib waveguide and a 340  $\mu$ m long adiabatic taper structure at each side. The demonstrated devices [see Fig. 3(b)] provide up to 6.5 dB on-chip gain at a bias current of 110 mA, as shown in Fig. 3(c).

## 2. Evanescently coupled DFB lasers

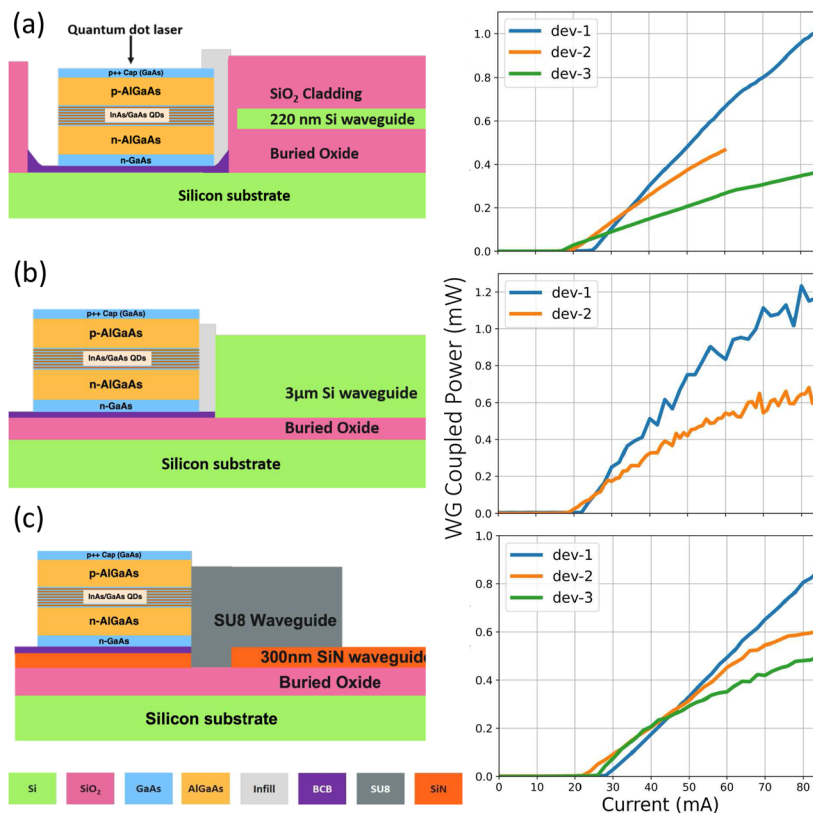
GaAs QD DFB lasers exhibit extra features of high-temperature stability, reduced sensitivity to external feedback, and low threshold current compared to quantum well (QW) lasers, making them suitable for use in uncooled integrated transceivers in data centers. Following the success of GaAs QD optical amplifiers, DFB lasers were also demonstrated on the imec SiPh platform. The layout and the dimensions of the DFB lasers are almost the same as for the aforementioned optical amplifier, except for the use of 1 mm long phase-shifted Bragg gratings defined in the crystalline Si waveguide, as the schematic layout illustrates in Fig. 4(a). The fabricated devices shown in Fig. 4(b) exhibited single-mode operation at 1300 nm with a 44 dB side-mode-suppression-ratio (SMSR), as shown in Fig. 4(c). The maximum single-side waveguide-coupled output power was measured to be 0.7 mW.<sup>34</sup>



**FIG. 4.** DFB lasers based on GaAs QD gain coupons. (a) Schematic layout of the DFB laser. (b) Microscope image of an array of resulting devices. (c) Recorded optical spectra at different bias currents (images from Ref. 34).

## 3. Edge-coupled Fabry-Pérot lasers

Edge coupling (or facet coupling) is another popular approach to interface two different waveguide circuits. Compared to the evanescently-coupled device, the edge-coupling does not require long adiabatic taper structures, at least in the III-V waveguide, for optical coupling. Figure 5 shows the integration of GaAs QD lasers on three different photonic platforms through edge coupling.<sup>49</sup> The imec iSiPP50G platform is used in the first demonstration, and the GaAs QD device coupon sits on a locally exposed Si substrate. The InAs/GaAs QD waveguide is leveled to the 220 nm thick Si waveguide by incorporating an n-cladding layer whose thickness is carefully calibrated to that of the buried SiO<sub>2</sub> layer, as depicted in Fig. 5(a). The Si waveguide width is tapered from 380 to 150 nm to expand the fundamental TE mode field to match that of the optical mode emitted from the laser. GaAs QD lasers with lengths of 1.8 and 2.4 mm were printed into the recesses with <500 nm lateral misalignment. The threshold currents of the transfer-printed devices are below 20 mA. However, suffering from a large air gap (>5  $\mu$ m) between the facets of the GaAs QD waveguide and the Si waveguide, the waveguide-coupled power at room temperature is limited to 1 mW at 80 mA. The cross-sectional dimensions of the Si waveguide in the second photonic platform are 3  $\times$  2.5  $\mu$ m<sup>2</sup>. 1.5 mm long device coupons were transfer-printed onto the buried oxide layer, with their output ports being aligned to the Si waveguide, as depicted in Fig. 5(b). The performance of these devices is similar to that observed in the first demonstration. The third demonstration shown in Fig. 5(c) showcases the integration of GaAs QD lasers



**FIG. 5.**  $\mu$ TP of edge-emitting GaAs QD F-P lasers: (a) on a 220 nm SiPh platform with back-end layer stack, (b) on a 3  $\mu$ m thick SiPh platform with air cladding, and (c) on a 300 nm thick SiN photonics platform (images from Ref. 49).

on SiN PICs using  $\mu$ TP, where 1.8 mm long devices were used. A SiN taper structure assisted by a SU-8 down coupler defined in the post-printing processes is used to couple the optical mode to the SiN waveguide in an evanescent manner. The thresholds of the printed devices are below 30 mA, and over 0.8 mW of waveguide-coupled power is obtained at room temperature, at 85 mA.

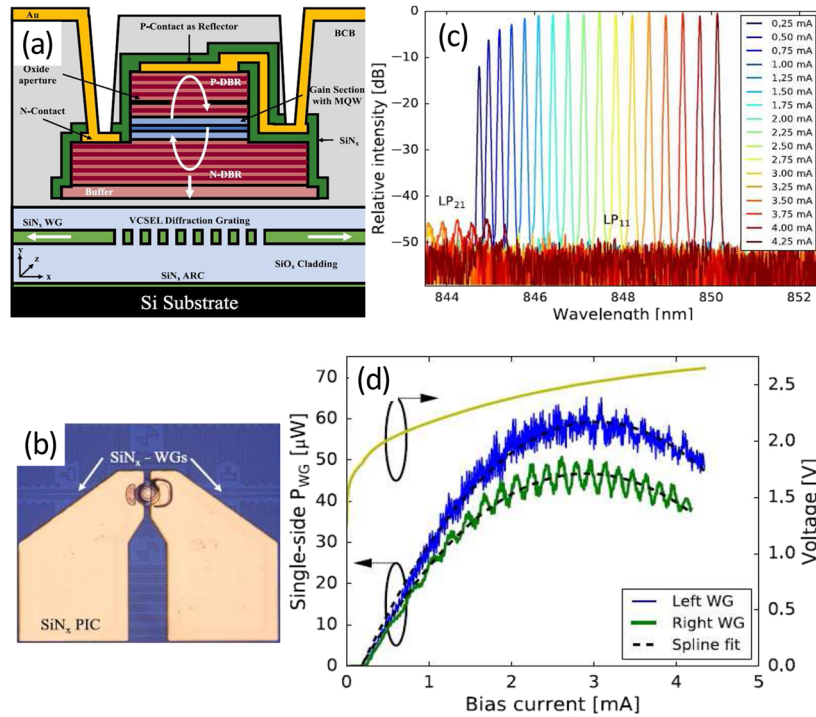
#### 4. VCSELS

The devices introduced in the above sections all have planar cavities with planar emission. Their active sections, or cavity lengths, all exceed 1 mm in length to obtain sufficient optical gain. Consequently, this is associated with elevated threshold currents and higher power consumption. Vertical-cavity surface-emitting lasers (VCSELS) feature very compact sizes, sub-mA thresholds, high wall-plug efficiencies, etc. These are promising devices that can heavily reduce the power consumption of photonic systems-on-chip. Another approach to greatly reduce power consumption and improve the performance of optical systems is by utilizing low-loss waveguide circuits. SiN photonics is outstanding in this aspect and shows much higher thermal stability compared to Si photonics. The demonstration shown in Fig. 6 successfully combines the advantages of VCSELS and SiN photonics with  $\mu$ TP pre-fabricated GaAs VCSELS on an imec BioPIX300 SiN platform.<sup>35</sup> As shown in Fig. 6(a), the VCSEL consists of a high reflectivity distributed Bragg

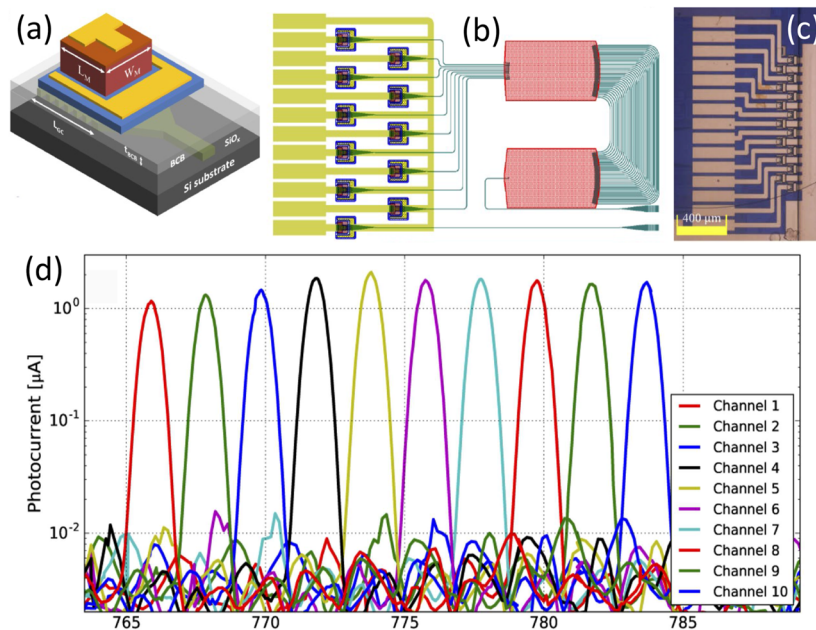
reflector (DBR) on top, a relatively lower reflectivity DBR mirror at the bottom, and an active region with five QWs in between. The laser emission is coupled to the underlying SiN waveguide through a diffraction grating that additionally introduces larger reflections for TE polarization. This lowers the TE polarization threshold relative to the TM polarization threshold and thereby enables single-polarization operation. Figure 6(b) shows a microscope image of a representative transfer-printed VCSEL. The integrated VCSEL devices exhibit single-mode operation with up to 45 dB SMSR at 850 nm, and over 5 nm wavelength tuning was realized by sweeping the bias current from 0.25 to 4.25 mA, as shown in Fig. 6(c). The threshold currents of the demonstrated devices are below 1 mA, and the maximum waveguide-coupled power is above 100  $\mu$ W, as shown in Fig. 6(d). Moreover, less than a 3 dB power reduction was observed when the temperature of the substrate increased from 25 to 85  $^{\circ}$ C.

#### 5. PIN photodiodes

In the previous section, we introduced the integration of optical sources operating around 850 nm. The demonstration discussed in this section deals with optical detection within that same wavelength range.<sup>14</sup> These photodiodes were fabricated on a source epitaxial wafer that consists of a 2.5  $\mu$ m thick GaAs intrinsic absorbing layer, a 300 nm thick p-doped GaAs top contact layer, and a 600 nm AlGaAs



**FIG. 6.**  $\mu$ TP of 850 nm GaAs VCSELs on SiN waveguide circuits. (a) Schematic layout of the VCSEL integrated on a SiN diffraction grating. (b) A microscope image of the resulting device. (c) Wavelength tuning behavior of a representative device. (d) Measured waveguide-coupled output power at the left and right waveguide ports (images from Ref. 35).



**FIG. 7.**  $\mu$ TP of GaAs p-i-n photodiodes on SiN waveguide circuits. (a) Schematic of the transfer-printed p-i-n photodiode on top of a SiN grating coupler. (b) A GDSII schematic of the spectrometer with an array of integrated GaAs photodiodes printed on the corresponding output grating couplers. (c) A microscope image of the resulting GaAs p-i-n photodiode array. (d) The measured photocurrent of the transfer-printed photodiodes (images from Ref. 14).



n-doped contact layer whose bandgap is designed to be 760 nm to avoid excess loss in the n-contact. In this work, ten photodiodes were aligned and printed onto a set of corresponding grating couplers within a SiN PIC realized on the imec BioPIX300 platform, as illustrated in Fig. 7(a). These grating couplers are linked to the output ports of an arrayed waveguide grating (AWG), as depicted in Fig. 7(b). The printed photodiodes [see Fig. 7(c)] exhibit 15 pA dark current and up to 0.3 A/W responsivity around 860 nm at 2 V reverse bias. All the printed devices operated similarly, and the recorded photocurrents perfectly reproduced the filter response of the AWG, as shown in Fig. 7(d), illustrating the feasibility of the integration of such photodiodes on a SiN photonics platform through  $\mu$ TP.

## 6. Single photon sources

Si quantum photonics holds promise for the realization of complex, high-performance quantum PICs for quantum communication, linear quantum computation, and quantum teleportation. Nonetheless, the current lack of deterministic, high-purity, and high-indistinguishability single-photon sources in Si presents a worrisome hurdle.<sup>50</sup> Amongst several proposed approaches,  $\mu$ TP of

III–V-based single photon sources (SPSs) is found to be a very promising method to cope with this issue. Three of these demonstrations are shown in Fig. 8. The first demonstration is based on the  $\mu$ TP of GaAs nanobeams on SiN PICs,<sup>51</sup> as shown in Fig. 8(a). The nanobeam is 120  $\mu$ m long and is defined in a 160 nm thick GaAs device layer that contains a layer of self-assembled InAs quantum dots for the generation of single photons. The printed device shows 3 dB excess loss, paving the way for the integration of SPSs. The demonstration shown in Fig. 8(b) relies on the  $\mu$ TP of one-dimensional (1D) photonic crystal (PhC) GaAs nanobeam cavities. Two devices were successfully integrated into a single Si waveguide, and the optical spectra obtained at the output ports reveal strong QD emissions at 900 and 904 nm from the devices.<sup>52</sup> The total single-photon coupling efficiency from the nanocavity to the underlying Si waveguide is estimated to be 70%. Given the symmetric structures of the aforementioned nanocavities, QD emissions are coupled to the Si waveguide in both directions, potentially limiting the efficiency of the integrated sources. By using a PhC mirror in the Si waveguide, unidirectional coupling of QD emission to the underlying waveguide was demonstrated,<sup>53</sup> as shown in Fig. 8(c). Furthermore, a sub-wavelength waveguide structure was incorporated into the Si waveguide to reduce the effective index and, consequently, relax the required alignment of the nanocavity with the mirror.

## 7. AlGaAs microdisk resonators

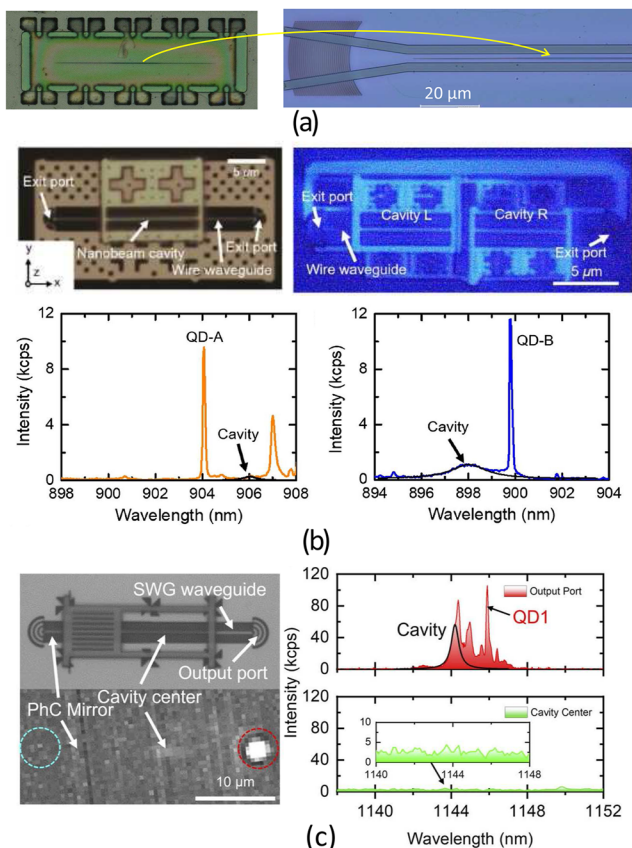
AlGaAs materials have outstanding second- and third-order nonlinearity along with low two-photon absorption. Integration of AlGaAs materials on SiPh platforms has been acknowledged as an effective approach to augmenting Si PICs with nonlinear optical functionalities. Figure 9 illustrates the integration of high-Q AlGaAs microdisks onto the SiPh platform using  $\mu$ TP. In the first case, a microdisk with a radius of 5  $\mu$ m is printed on top of the buried oxide, next to the Si waveguide.<sup>33</sup> The microdisks were defined in a 270 nm thick  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$  device layer and released from the GaAs substrate by selectively etching a 500 nm thick AlAs sacrificial layer in between. The microdisk was well aligned to the underlying Si waveguide to have sufficient optical coupling to the Si waveguide. A loaded Q-factor of 7000 was obtained in the measurement, as shown in Fig. 9(a). In the second case, the microdisks were printed on top of the Si waveguides, which have been planarized with a 250 nm thick hydrogen silsesquioxane (HSQ) upper cladding, as shown in Fig. 9(b).<sup>54</sup> A 500 nm thick  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$  sacrificial layer was used to release the micro-disks. Up to 40 000 loaded Q-factors were obtained for a 5  $\mu$ m radius device. A nonlinear coefficient of  $325 \text{ mW}^{-1}$  with a four-wave mixing (FWM) efficiency of  $-24.9 \text{ dB}$  at an on-chip pump power of 2.5 mW was obtained in a FWM experiment.

## B. InP

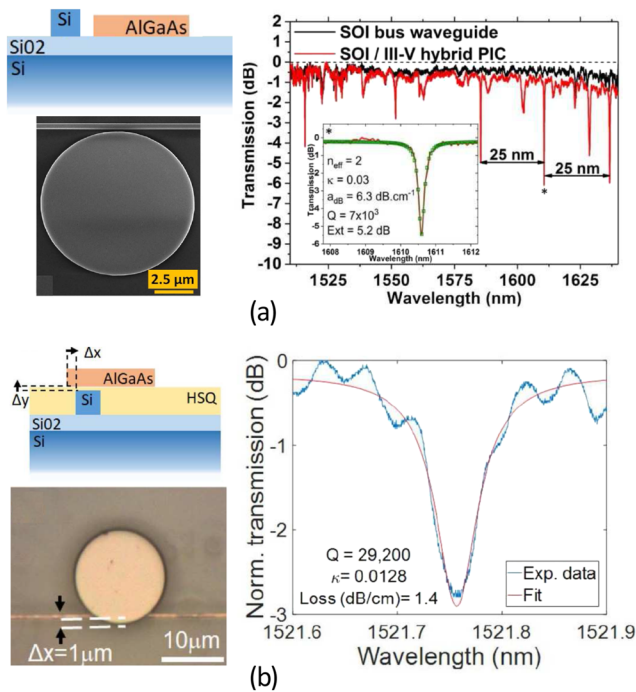
In this section, several demonstrations will be discussed that rely on the printing of InP coupons on SOI or SiN. The devices that will be presented are DFB, tunable, mode-locked, nanobeam cavity lasers, and UTC photodetectors.

### 1. Evanescently coupled DFB lasers

In the past couple of years, our own research has demonstrated several C-band III–V-on-Si DFB lasers that rely on the printing of InP gain coupons on DFB gratings that are defined in the Si device



**FIG. 8.**  $\mu$ TP of SPSs on SiPh substrates. (a)  $\mu$ TP of a GaAs nanobeam on top of a SiN waveguide. (b)  $\mu$ TP of two GaAs nanocavity SPSs on a single Si waveguide circuit. (c) Transfer-printed GaAs SPS on Si with unidirectional output (images from Refs. 51–53).

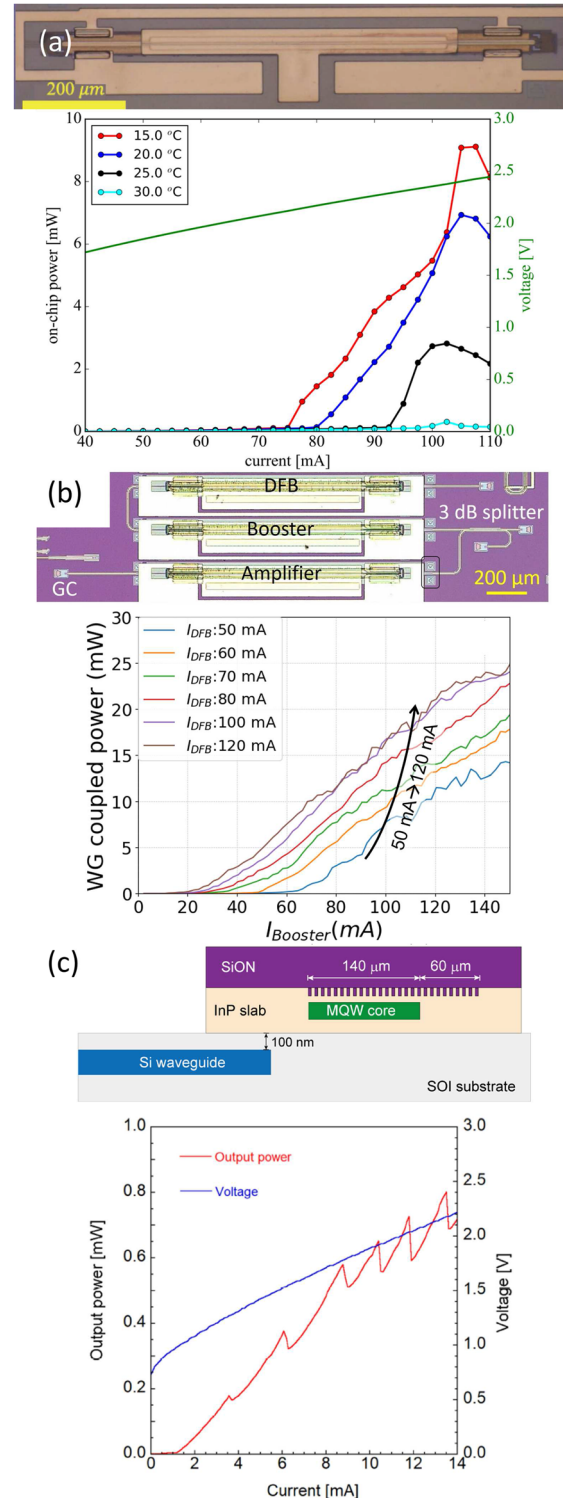


**FIG. 9.**  $\mu$ TP of AlGaAs microdisks. (a) AlGaAs microdisk adjacent to a Si waveguide. (b) AlGaAs microdisk on top of a Si waveguide (images from Refs. 33 and 54).

layer of the target wafer. The SiPh platform used for these implementations is an SOI platform with a 400 nm thick Si device layer. Single mode C-band operation has been realized with these devices. 7 mW of waveguide-coupled output power at 20 °C is obtained.<sup>55</sup> This laser source, shown in Fig. 10(a), offers a SMSR above 33 dB, has a threshold current of 80 mA, and lases at 1558 nm. A slope efficiency of 0.27 W/A was achieved at 20 °C.

To overcome the output power limitations of this III-V-on-Si DFB laser, two identical InP SOA coupons can be printed, individually or in a single array printing step, on an SOI integrated circuit where the printing site for the first SOA contains a DFB grating while the printing site of the second SOA is designed in such a way that this printed coupon behaves as a power amplifier.<sup>56</sup> This III-V-on-Si DFB laser with a co-integrated power amplifier was shown to provide single mode operation around 1540 nm at 20 °C and is depicted in Fig. 10(b). A waveguide-coupled output power of 14 dBm could be achieved with 28 dB SMSR at a total bias current (DFB + power amplifier) of 270 mA. The maximum wall-plug efficiency that could be achieved is about 4%.

Recently, membrane distributed reflector (DR) lasers were demonstrated based on the  $\mu$ TP technique.<sup>57</sup> Membrane coupons are very thin and, therefore, allow for easier optical coupling to the underlying Si waveguide. In addition, membrane lasers relying on lateral p-i-n diodes provide high optical confinement. Consequently, such membrane lasers have a low threshold current and are compatible with low-energy, high-speed optical input-output (I/O) links through direct modulation. The membrane distributed reflector laser described in Ref. 57 offers single-mode operation at



**FIG. 10.** DFB lasers based on InP gain coupons: (a) on a 400 nm SOI platform, grating in the SOI; (b) same as (a) but with a co-integrated power amplifier; and (c) membrane laser on a 220 nm SOI with grating defined on the source (images from Refs. 55–57).

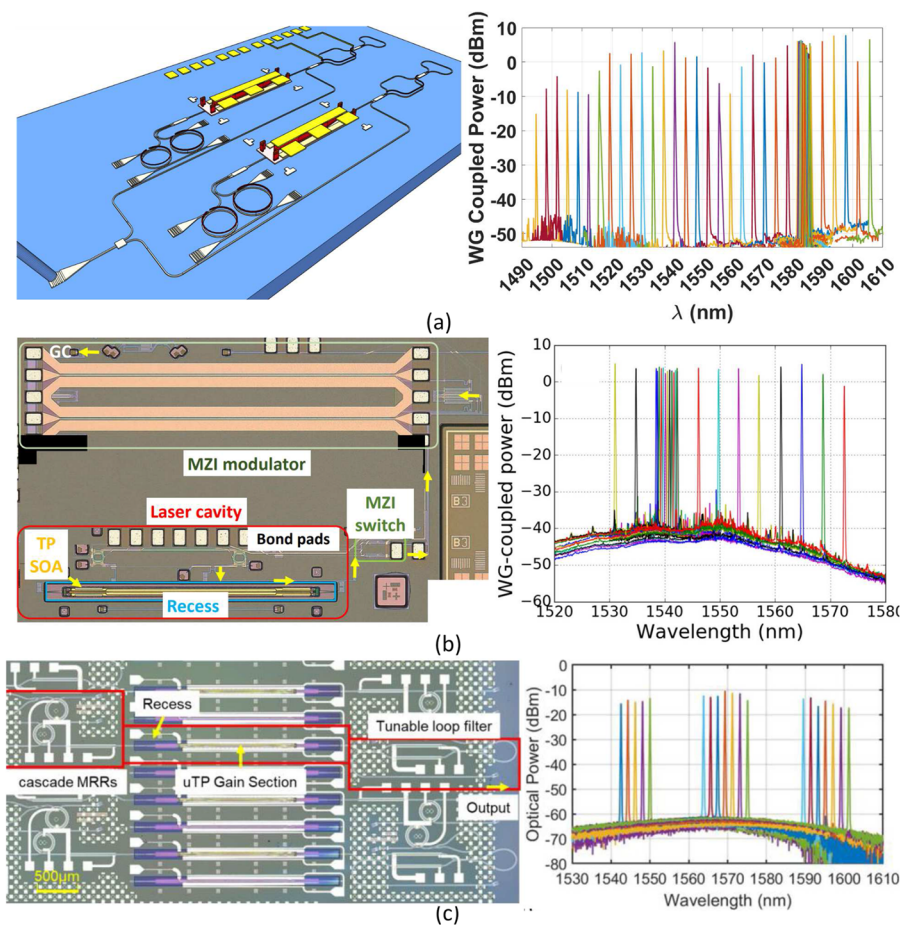
1535 nm, has a SMSR of 40 dB at 14 mA bias, a threshold current of only 1.2 mA, and a maximum output power of 0.8 mW. Direct modulation of the laser shows an electro-optical bandwidth beyond 25 GHz with which 50 Gb/s nonreturn to zero (NRZ) signals with an extinction ratio of 2.5 dB could be transmitted. The target SiPh platform used for the demonstration is a 220 nm SOI platform, and, in contrast to the above DFB lasers, it requires the definition of the DFB and distributed Bragg reflector (DBR) section of the laser already on the source wafer, as shown in Fig. 10(c).

## 2. Widely tunable C-band lasers

$\mu$ TP has also been used for the realization of integrated, widely tunable lasers on SOI and SiN platforms. In this section, we will cover three of our C-band, widely tunable laser demonstrations. Because of the large optical gain bandwidth of the InP amplifiers, Vernier filters are required to establish single mode operation. The first demonstration that will be discussed is an S+C+L band widely tunable double laser structure, visualized in Fig. 11(a), that has a combined 110 nm tuning range.<sup>29</sup> The pick-up laser relies on the printing of two types of III-V SOAs on a 400 nm SOI platform. The

two SOA types have gain peaks at, respectively, 1525 and 1575 nm and are printed on two laser cavities defined in the SiPh target wafer. Each of these laser cavities contains a Vernier filter and has a tunable loop mirror at the output. Subsequently, the two laser outputs are combined in the Si PIC toward a single fiber output. With the dual-laser approach, the output wavelength of the combined laser can be tuned from  $\sim$ 1495 to 1605 nm. Narrow linewidth operation was observed, and the frequency noise threshold mask defined by the OIF-400-ZR standard for coherent optical transceivers was met over the entire tuning range. At 1530 nm, a Lorentzian linewidth of about 20 kHz was achieved.

The second device is an integrated transmitter<sup>58</sup> that comprises not only a widely tunable laser but also a co-integrated Mach-Zehnder modulator (MZM). The integrated transmitter is shown in Fig. 11(b), where the laser ring cavity and Si-doped MZM were implemented on imec's 220 nm SOI platform, iSiPP50G. Whereas the first laser demonstration was realized on a 400 nm SOI platform, the Si thickness on many SiPh platforms is typically only 220 nm, thereby hindering the efficient coupling between the Si waveguide and the III-V active layer. To enhance the coupling



**FIG. 11.** Widely tunable lasers based on InP gain coupons. (a) 110 nm tuning range double-laser device on a 400 nm SOI platform, (b) integrated 40 Gb/s transmitter with 40 nm tuning range on a 220 nm SOI platform, and (c) 60 nm tuning range narrow-linewidth laser on a SiN platform (images from Refs. 29, 58, and 59).



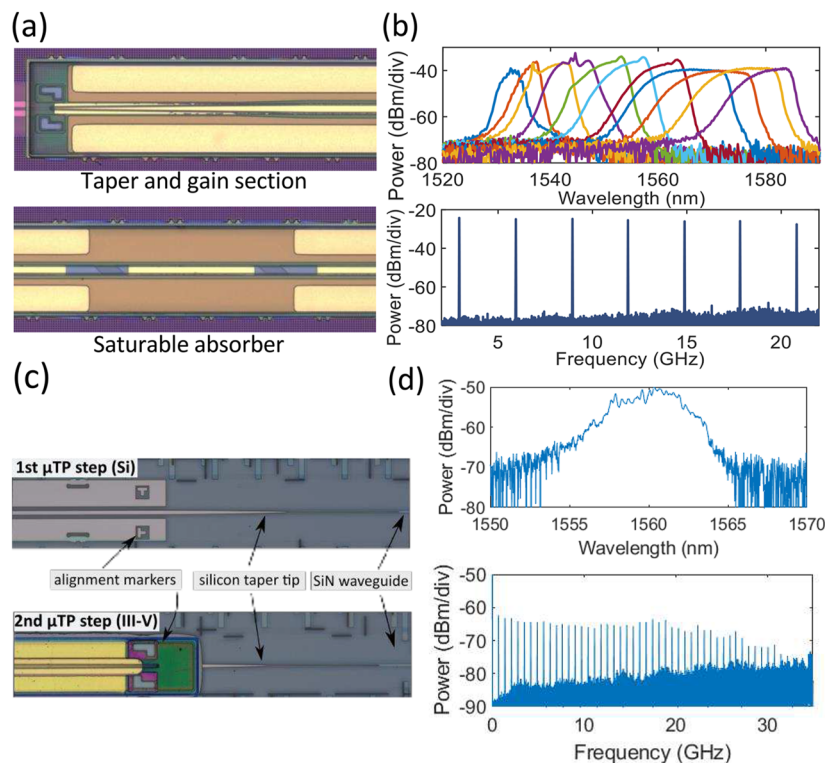
while still using the 220 nm Si waveguides elsewhere in the integrated circuit, the Si waveguide layer is tapered locally to a thicker poly-Si-on-Si hybrid waveguide. Single-mode lasing with an over 40 nm tuning range was achieved, and in combination with the MZM, the integrated transmitter is capable of transmitting 40 Gb/s non-return-to-zero (NRZ) in the C-band.

For the final demonstration of InP based widely tunable lasers, InP gain coupons were printed on an amorphous-Si/Si<sub>3</sub>N<sub>4</sub> platform.<sup>59</sup> By making use of the low-loss property of SiN waveguides in combination with high-Q ring resonators, kHz-level linewidths can be achieved. The amorphous Si in this platform serves as a bridging layer between the Si<sub>3</sub>N<sub>4</sub> waveguides and the InP active layer, thereby enabling efficient coupling between the two. The demonstrated laser, shown in Fig. 11(c), offers a 0.36 mW fiber coupled output power at 124 mA bias current, or equivalently 1.5 mW waveguide-coupled output power. Tuning of the lasing wavelength was demonstrated over 60 nm in the C+L band. Single-mode lasing with a SMSR of at least 40 dB was achieved over the entire tuning range, and linewidths down to about 3 kHz were obtained with this device.

### 3. Mode-locked lasers

Integrated mode-locked lasers find applications across various fields, such as distance measurements, spectroscopy, telecommunications, and bio-sensing. While efficient fiber or bulk lasers are

commonly used in those systems, there is a growing interest in on-chip solutions due to their potential for cost reduction and compact footprint. Integration of gain on SiPh, and more particularly on low-loss SiN, using  $\mu$ TP is a suitable solution to build such mode-locked lasers. In that case, the coupling from the circuit to the amplifier is done via an intermediate Si layer to overcome the large refractive index difference between the SiN and the amplifier stack.<sup>60</sup> The gain section is composed of InAlGaAs periodically grown layers forming a multiple-quantum-well<sup>25</sup> in between n-type and p-type indium phosphide cladding layers and includes a saturable absorber section to allow the mode-locking operation. The first demonstrations have been done using a customized platform, including amorphous or crystalline Si interlayers.<sup>61–63</sup> The use of a passive low-loss SiN extended cavity allows, in those cases, to obtain low noise lasers showing an optical linewidth below 1 MHz. By optimizing the design and refining the hybrid amorphous Si to III–V mode overlap, mode-locked lasers with a wide region of stability in view of the laser biasing parameters (gain current and saturable absorber voltage) have been demonstrated. Furthermore, by tuning the driving parameters, the center wavelength of the optical comb can be shifted over 50 nm. This laser is presented in Figs. 12(a) and 12(b). In another work, the intermediate coupling Si layer is transfer printed in order to make possible the use of a commercial SiN platform, as shown in Figs. 12(c) and 12(d), reducing the complexity and cost of the passive cavity fabrication.<sup>64</sup>



**FIG. 12.** Overview of mode-locked lasers. (a) Mode-locked laser using an amorphous Si intermediate coupling layer. (b) Optical and electrical spectra when mode-locking. (c) Printing and patterning of a Si coupon on a SiN circuit serving as an intermediate adiabatic coupling layer and picture of the laser. (d) Corresponding optical and electrical spectra when mode-locking the laser.

#### 4. Single photon sources

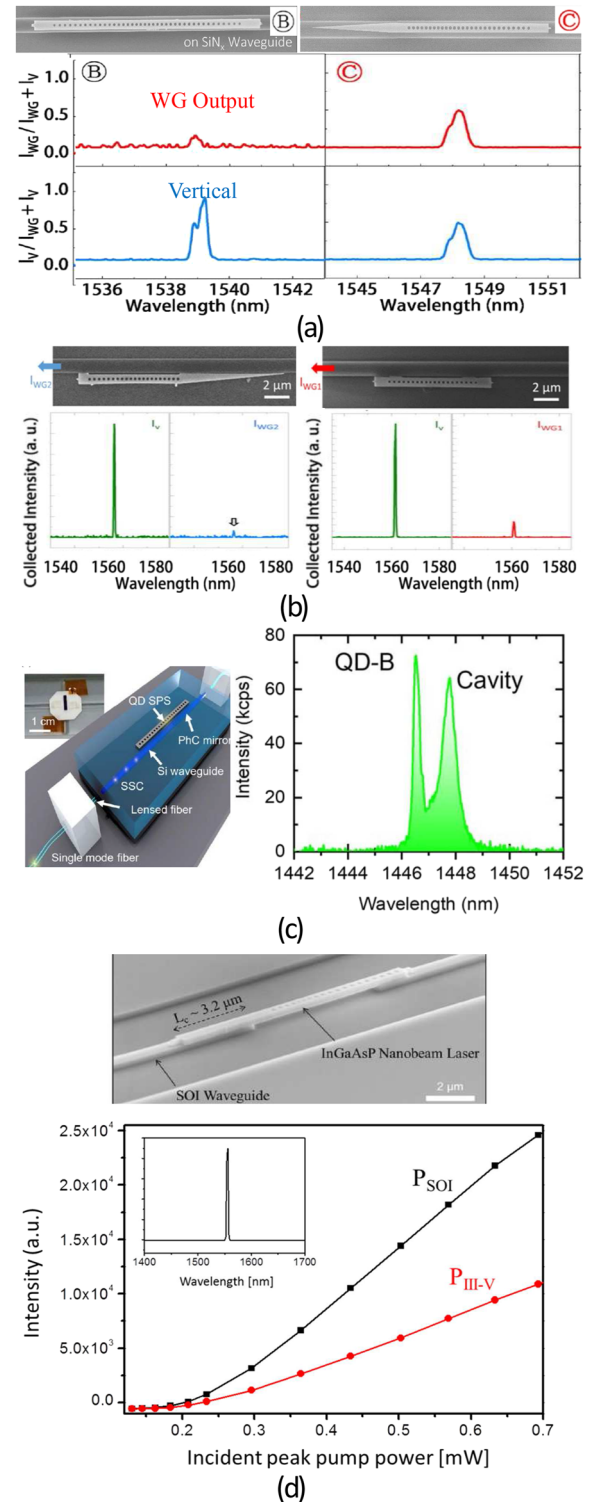
Several InP-based nanobeam cavity lasers have been reported over the past years. These can play a key role in quantum networks such as C-band SPSs. Four of these demonstrations are shown in Fig. 13. (a),<sup>65</sup> (b),<sup>66</sup> and (d)<sup>67</sup> rely on the printing of an InGaAsP photonic crystal nanobeam cavity on SiPh, while the nanobeam in (c)<sup>68</sup> is made out of InP with InAs QDs. It needs to be mentioned that the demonstrations shown in (a) and (b) were made by the same group, but the second device uses a docking approach to improve the alignment accuracy by using the SiN waveguide as a mechanical stop.<sup>65,66</sup>

The nanobeam laser shown in Fig. 13(a) has a threshold of 180  $\mu\text{W}$  and a unidirectional coupling efficiency in excess of 50%. The nanobeam laser relying on  $\mu\text{TP}$  with docking offers a unidirectional coupling efficiency of around 65%. Furthermore, this docking introduces improved integration of nano-beams on Si PICs. While demonstrations (a) and (b) are printed on SiN waveguides, the remaining two demonstrations are printed on SOI. Demonstration (d) again uses InGaAsP nanobeams; however, device (c) relies on an InAs/InP QD SPS and operates outside the C-band (at around 1436 nm). For this InAs/InP SPS, the single-photon coupling efficiency from QD to the SOI waveguide will be  $\sim 82\%$ , which can potentially be increased to 97.6% when including a photonic cavity mirror in the waveguide. Finally, the device shown in Fig. 13(d) achieved a coupling efficiency of 83% from the nanobeam laser to the SOI waveguide, with a lasing threshold and wavelength of around 200  $\mu\text{W}$  and 1556 nm, respectively.

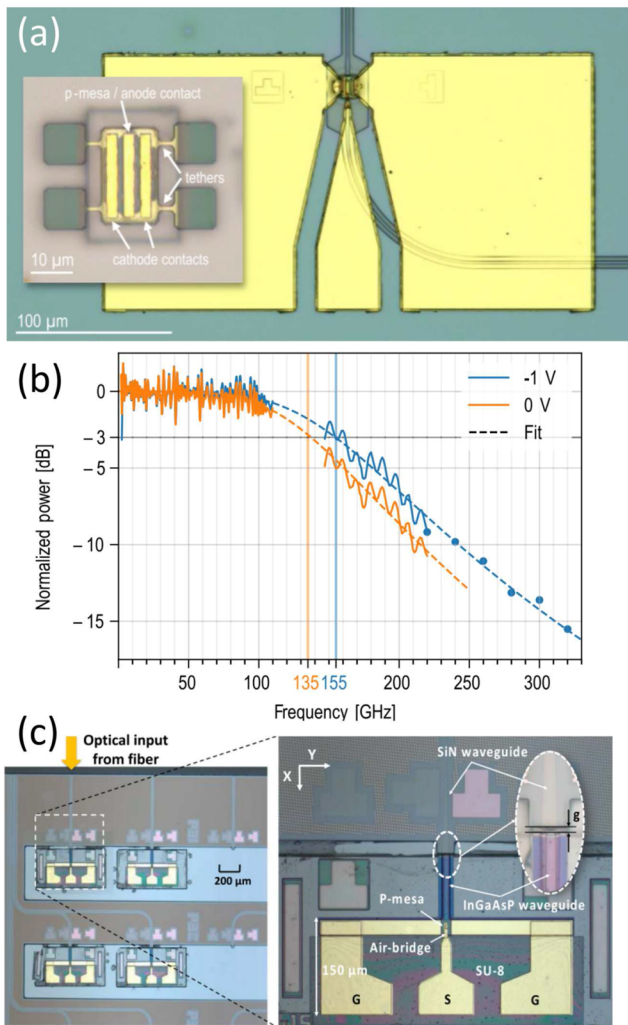
#### 5. UTC photodiodes

Now that several light sources have been discussed, it also needs to be mentioned that InP is also a suitable material for implementing photodiodes in the C-band. Recently, a unidirectional carrier photodiode (UTC-PD) was demonstrated where printing was done on a SiN platform.<sup>69</sup> In UTC-PD, carrier transport is limited to high-mobility electrons. Consequently, photodiodes relying on this technique offer much higher transit-time bandwidths. As an added benefit, this also improves power handling by limiting the space-charge screening effects.  $\mu\text{TP}$  of UTC-PD implies that very small coupons less than 100  $\mu\text{m}$  in size are to be printed. The printed devices resulted in a waveguide-coupled photodiode with a responsivity of 0.3 A/W at 1550 nm. At 0 V bias, a 3 dB bandwidth of 135 GHz can be reached, with bandwidths going to 155 GHz at  $-1$  V bias. The dark and saturation currents of this device are 10 nA and 4.5 mA, respectively. Finally, a back-to-back THz link was set up for a 300 GHz carrier, resulting in data rates up to 160 GB/s.<sup>69</sup> A microscope image of this printed UTC-PD, together with its frequency response, is displayed in Figs. 14(a) and 14(b).

In another demonstration, shown in Fig. 13(c), InGaAsP-based modified-UTC (MUTC) photodetectors were transfer printed in recesses and, in this way, butt-coupled with a SiN waveguide while the photodetector itself contained a short InGaAsP access waveguide.<sup>70</sup> This device results in 54 GHz bandwidth, 30 nA dark current at  $-3$  V, 0.42 A/W responsivity at 1310 nm, and high power handling at microwave frequencies. It can reach RF output powers up to 7 dBm at 50 GHz, while the 1 dB compression current is on average 22 mA.



**FIG. 13.** Transfer-printed nanobeam cavity lasers. (a) InGaAsP photonic crystal nanobeam on SiN waveguide. (b) Similar as (a) but by making use of mechanical docking. (c) InAs/InP QD nanobeam on SOI. (d) InGaAsP photonic crystal nanobeam on SOI waveguide (images from Refs. 65–68).



**FIG. 14.** (a) Microscope image of an evanescently coupled InP UTC photodiode at C-band. (b) Frequency response of (a) with a  $2 \times 12 \mu\text{m}^2$  active region. (c) Butt-coupled MUTC photodiode (image from Refs. 69 and 70).

### C. GaSb

For spectroscopic sensing applications, including greenhouse gas emission sensing and blood bio-molecule monitoring, fingerprints of the absorption spectrum need to be observed. This typically requires operating wavelengths between 2 and  $3 \mu\text{m}$ . Consequently, gain elements, laser sources, and photodetectors need to be devised in this short-wave-IR wavelength range. A recent demonstration<sup>71</sup> using a quantum well GaSb micro-transfer printed membrane reflective semiconductor optical amplifier (RSOA) in combination with a distributed Bragg reflector defined in an SOI platform showed an external cavity laser with a single emission frequency working at  $1.96 \mu\text{m}$ . This GaSb-on-SOI laser is shown in Fig. 15(a).

Furthermore, we are working on the  $\mu\text{TP}$  of GaSb coupons on a Ge-on-SOI platform. On this platform, germanium serves as a

bridging layer for efficient adiabatic coupling between Si and GaSb. Recently,<sup>72</sup> the required passives for implementing a heterogeneously integrated tunable laser (waveguides, microring resonators (MRRs), and Vernier filters) were demonstrated on the aforementioned Ge-on-SOI platform, together with a printing experiment of these coupons on the Ge-on-SOI waveguides. These GaSb SOA coupons before and after printing are shown in Fig. 15(b).

### D. Silicon

#### 1. Photonic Si devices

Integration of active devices on a SiN platform has seen considerable progress; however, these efforts are mainly targeting the telecom wavelength range. Meanwhile, for biosensing and imaging applications, the visible/near-infrared spectrum plays a key role. While the SiN platform itself is well suited for these wavelengths, demonstrations integrating sub-850 nm light sources and detectors on SiN PICs are scarce. Recently, Si p-i-n photodetectors were micro-transfer printed on a commercially available SiN platform to enable operation below 850 nm.<sup>37</sup> The demonstrated photodetectors [Fig. 16(a)] showed a responsivity of around  $0.19 \text{ A/W}$ , or equivalently 30% quantum efficiency, at 775–800 nm when using a  $-3 \text{ V}$  bias. Furthermore, this device provides a dark current and bandwidth of, respectively,  $107 \text{ pA}$  and  $6 \text{ GHz}$  at  $-3 \text{ V}$ , where the bandwidth is currently RC-limited.

Demonstrations showcasing the potential of printing Si coupons on SiPh targets are not limited to active devices. Printing Si membranes with predefined passive structures has been explored as well, as shown in Fig. 16(b). As an example of this technique, microring resonators have been implemented by printing Si membranes with a predefined ring on top of an SOI waveguide.<sup>73</sup> This approach potentially allows for the fabrication of multi-layer 3D photonic integrated circuits, offering benefits in both footprint and achievable complexity.

#### 2. Si electronics chipllets

Whereas most of the demonstrations in this review paper offer optical or opto-electronic functionalities,  $\mu\text{TP}$  is a flexible technique that can also be adopted for integrating the drive, receive, or control electronics that need to interface with the integrated photonics.  $\mu\text{TP}$  of electronic devices works in a similar fashion as photonic devices in the sense of relying on the existence of a sacrificial layer in the device stack that can be used to release the electronic chipllets from their native substrate, after which they are picked up and printed onto the SiPh target wafer. This technique has been demonstrated<sup>74</sup> where compact electronic ICs, fabricated in a  $130 \text{ nm}$  SiGe BiCMOS technology, have been accurately printed onto a SiPh wafer using a thin BCB layer ( $\leq 200 \text{ nm}$ ), providing a yield of over 90%. Such a printed electronic chipllet is shown in Fig. 16(c). During the post-processing of these heterogeneously integrated electro-optical circuits, metal interconnections can be defined. Using such on-chip metal traces rather than the nowadays often used wire-bonds or flip-chip bonds can help to significantly reduce the interconnection length, offering advantages in device performance, such as higher bandwidth and lower power consumption, and in the assembly flow, such as reduced costs and increased throughput.

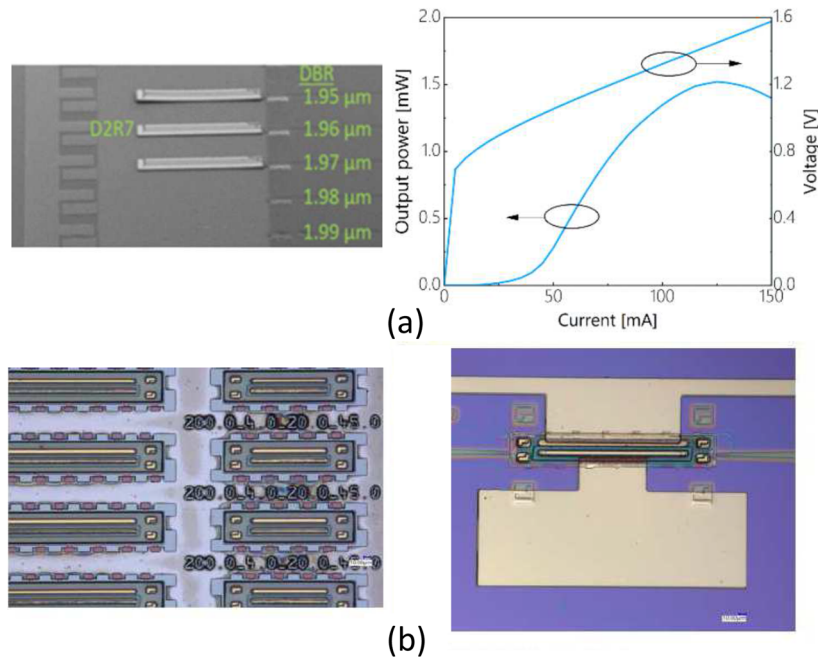


FIG. 15. (a) External cavity laser based on GaSb-on-SOI and (b) GaSb-on-Ge-on-SOI printing (images from Refs. 71 and 72).

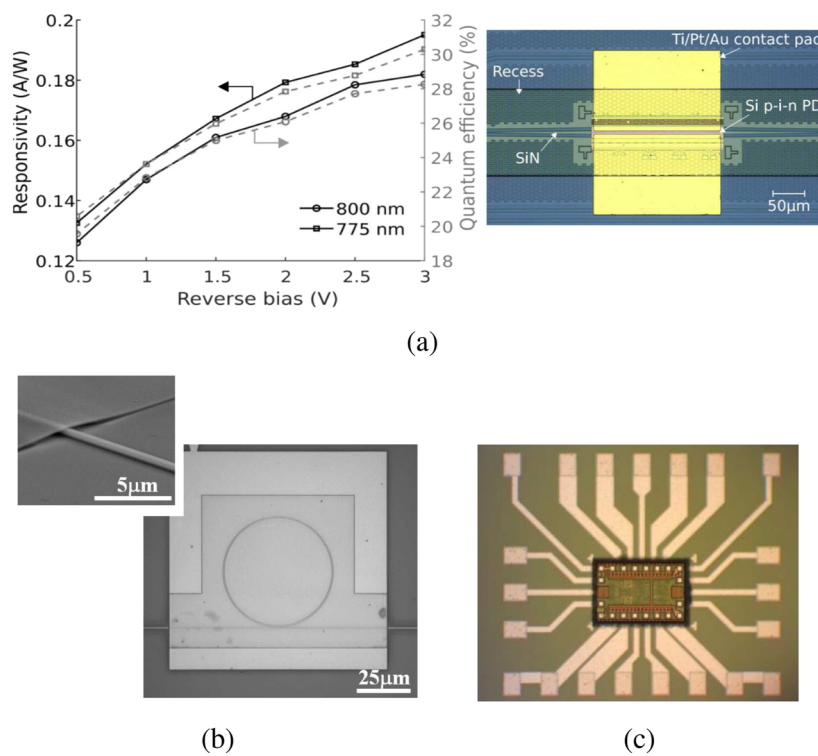


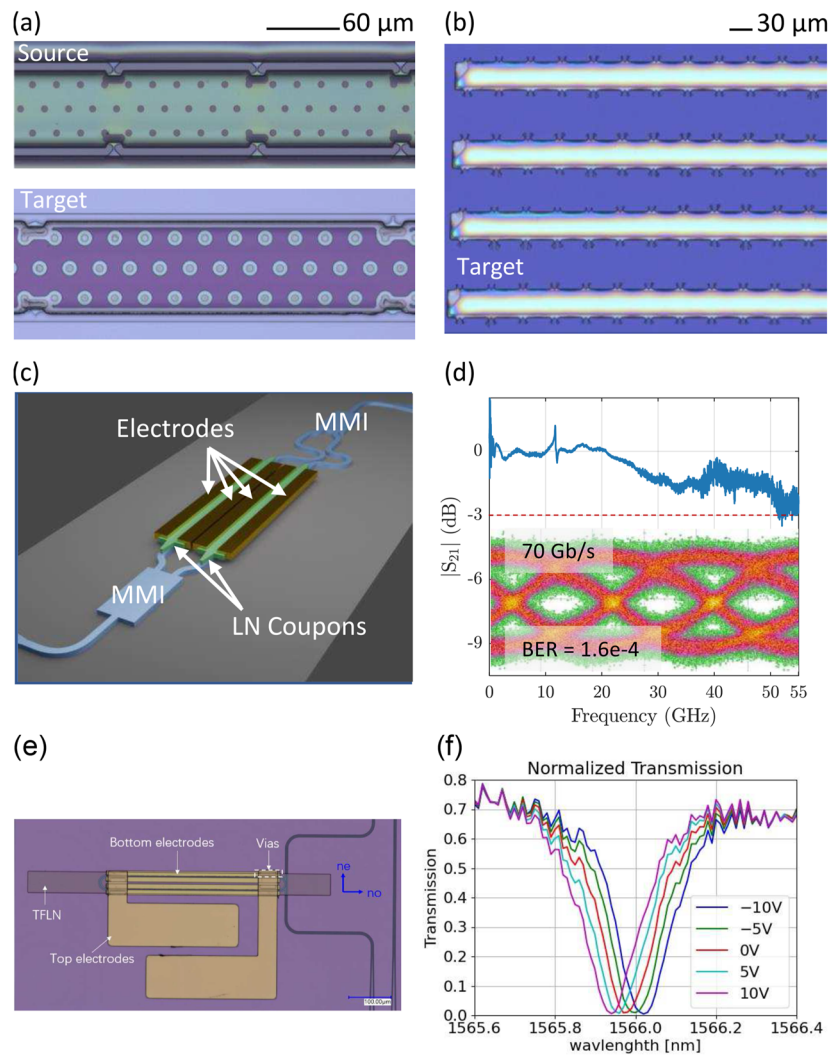
FIG. 16. Transfer printed Si devices: (a) near-visible photodetector, (b) microring membranes, and (c) electronic chiplets (images from Refs. 37, 73, and 74).



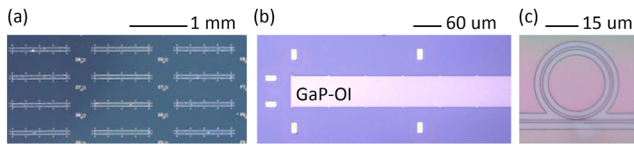
### E. Lithium niobate

Thin-film lithium niobate (LN)-on-insulator is a promising platform for integrated photonics. Indeed, the material properties of LN, including a wide transparency window (0.4–5  $\mu\text{m}$ ), combined with a strong second-order nonlinearity and electro-optic effect, make it suitable for several functionalities, such as frequency conversion, electro-optic frequency comb generation, or fast electro-optic modulation. Thin-film LN-on-insulator low-loss platforms have been widely reported in the literature, but there is a growing interest in the heterogeneous integration of thin films of LN using  $\mu\text{TP}$  on CMOS compatible platforms.<sup>75</sup> For LN systems, the  $\text{SiO}_2$  release layer is wet etched in a hydrofluoric acid based chemical solution, making the use of regular SiN encapsulation difficult. To overcome that issue, demonstrations of coupon suspension have been done with the help of photoresist encapsulation or using LN tether

structures. An advanced design of coupons based on pillar-based mechanical support, also helping to avoid photoresist delamination and suspension of large footprint areas, has been developed.<sup>76,77</sup> The coupons before and after printing can be seen in Fig. 17(a). However, the printing of such coupons requires a dedicated patterned target fitting the pillars.<sup>77</sup> A version of coupons excluding such pillars is also being studied but is asking for a more complex release process. An example of the mentioned coupons after  $\mu\text{TP}$  is shown in Fig. 17(b). This makes possible the use of LN coupons on regular planarized targets. As a proof of concept, several devices using transfer printed thin-film LN have been demonstrated, including fast modulators with a cut-off frequency above 55 GHz<sup>40,78</sup> [see Figs. 17(c) and 17(d)], LN-on-Si microring modulators<sup>79</sup> [see Figs. 17(e) and 17(f)], hybrid microring resonators on SiN with a Q-factor of 32 000,<sup>39</sup> hybrid SiN micro-cavities with a Q-factor of 50 000,<sup>80</sup> and



**FIG. 17.** Overview of LN  $\mu\text{TP}$ . (a) Pillar-based  $\mu\text{TP}$  of LN. (b)  $\mu\text{TP}$  of photoresist encapsulated LN coupons. (c) Fast MZM using transfer printed LN. (d) Frequency response of the modulator from figure (c). (e) Transfer-printed Si-LN microring modulator. (f) Wavelength tuning behavior of the micro-ring modulator from figure (e).



**FIG. 18.** Overview of GaP  $\mu$ TP. (a) Picture of GaP printed coupons. (b) GaP-on-insulator (GaP-OI) thin film before patterning. (c) GaP-on-insulator thin film after patterning.

periodically-poled waveguides for second harmonic generation.<sup>81</sup> Integration of such devices with a high yield could make possible the use of LN in photonic chips fabricated in CMOS foundries as a back-end level process in order to offer new complementary functionalities to the platforms.

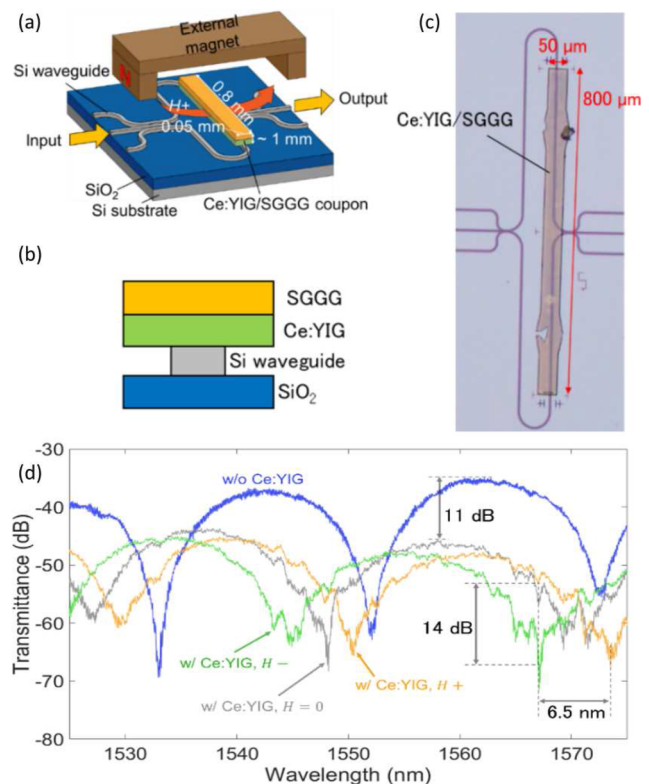
## F. Gallium phosphide

Gallium phosphide (GaP)-on-insulator is a suitable candidate for on-chip nonlinear photonics due to the excellent properties of GaP, which include a large optical transparency window (0.55–11  $\mu$ m) and strong second and third order nonlinearities. Low-loss GaP-on-insulator fabricated by die-to-wafer bonding that allows for Kerr frequency comb generation has been reported.<sup>82,83</sup> In the case of GaP, the substrate removal after bonding is not trivial and requires selective inductively coupled plasma (ICP) dry etching. Another way of hetero-integrating is to transfer print the material directly on an insulator. For that, the material coupons are patterned, encapsulated in amorphous Si or photoresist, released, and transferred to the target, as illustrated in Figs. 18(a) and 18(b). As a proof of concept, microring resonators [Fig. 18(c)] with a Q-factor of 35 000 have been demonstrated.<sup>36,84</sup> Large-footprint thin films of GaP printed using the pillar-assisted method are also reported.<sup>77</sup> Next, we want to use transfer printed devices to demonstrate their use in nonlinear applications, such as supercontinuum and comb generation.

## G. Ce:YIG

The  $\mu$ TP of magneto-optical films can be leveraged to introduce non-reciprocal functionalities in integrated photonics. Integrated optical isolators can play a key role in enhancing the performance and improving the stability of on-chip integrated laser sources by strongly suppressing the back-reflection into the laser cavity. In addition, integrated optical circulators can be used in a variety of applications, including full-duplex communication links and integrated optical sensors.

Cerium-substituted yttrium iron garnet ( $\text{Ce}_1\text{Y}_2\text{Fe}_5\text{O}_{12}$ , abbreviated as Ce:YIG) introduces a large Faraday rotation coefficient at telecommunication wavelengths, i.e.,  $-4500^\circ/\text{cm}$  at 1500 nm, making this a suitable material platform to implement compact on-chip magneto-optic devices.<sup>44</sup> Recently, a Mach-Zehnder interferometer (MZI) based magneto-optic isolator was demonstrated by  $\mu$ TP Ce:YIG/substituted gadolinium gallium garnet (SGGG) coupons on Si waveguides,<sup>44</sup> where SGGG (substituted gadolinium gallium garnet) is the growth substrate. This reported isolator, shown in Fig. 19, based on the magneto-optic Kerr effect, has a footprint of  $0.25 \text{ mm}^2$  and achieves a maximum isolation ratio of 14 dB at 1567.1 nm,



**FIG. 19.** Optical isolator by  $\mu$ TP Ce:YIG films on SOI. (a) Isolator operation with an external magnet and Ce:YIG coupon on a SOI MZI. (b) Cross-section view. (c) Microscope image of the fabricated isolator. (d) Transmission of the MZI with and without  $\mu$ TP Ce:YIG coupon, with and without an external magnetic field (images from Ref. 44).

where the dimensions of the Ce:YIG coupon are  $50 \times 800 \mu\text{m}^2$  with a thickness of  $\sim 1 \mu\text{m}$ .

## H. Diamond

Single crystalline diamond (SCD) films, when integrated on a low-index substrate, can realize highly confined optical fields in the SCD, thereby introducing strong light-matter interactions, which can play a key role in several demonstrations, such as on-chip quantum optics, optomechanics, and non-linear optics.  $\mu$ TP of prepatterned SCD microdisks (not requiring a release layer) on SOI waveguides has been demonstrated<sup>45</sup> in an adhesiveless fashion. Loaded Q-factors of 31k on average were demonstrated. Because of the large thermal isolation imposed by the  $\text{SiO}_2$  in between the SCD and the Si waveguides, continuous resonant wavelength tuning of the microdisk over 450 pm is possible with an optical pump of 4.25 mW.

## III. WHAT IS AHEAD?

The current achievements in fabricating heterogeneous PICs through  $\mu$ TP are proof-of-concept demonstrations. Several steps need to be taken for the commercial uptake of the technology in the field of PICs. This forms the roadmap for the developments at



Ghent University–imec. The first aspect that needs to be tackled is proving the high yield of the  $\mu$ TP process. This yield comprises several aspects: the yield of the devices on the source wafer, including the release process, the yield of the pick-up process, and the yield of the printing process. The latter includes alignment accuracy and the absence of voids (due to particles) at the bonding interface. As for the yield of devices on the source wafer, this requires running source wafers in established foundries, be it for III–V semiconductors, Si, LiNbO<sub>3</sub>, or other materials. We are actively engaging with such foundries to transfer our source wafer processes. This yield can be improved by only transferring known-good devices. However, it is an economical question whether the cost of testing and inspection of the devices prior to integration makes up for the cost of the yield loss. The release process yield is determined by the fraction of devices that collapse onto the substrate after etching the release layer. In most cases, so far, wet chemistry is used to etch the release layer, which can cause collapse during drying because of capillary forces. In some cases, this issue can be circumvented by using vapor phase etching processes, such as vapor HF (using SiO<sub>2</sub> as the release layer) or vapor XeF<sub>2</sub> (using Si as the release layer). This yield also strongly relates to the strength and number of tethers supporting the devices and is, in that sense, also related to the pick-up yield: on the one hand, one wants the tethers to be strong enough for the devices not to collapse on the substrate, but on the other hand, they should also not be too strong to prevent a yield hit in the pick-up process (i.e., breaking of the tethers). Finally, the printing yield involves the printing of the coupons within the required alignment accuracy and without voids present at the bonding interface. State-of-the-art  $\mu$ TP tools offer an alignment accuracy of  $\pm 0.5 \mu\text{m}$   $3\sigma$  when printing large arrays of devices, so the optical interface between the coupons and the target waveguide circuit needs to be designed such that it can support such a misalignment. A bigger concern is voids at the bonding interface, typically due to particles. This becomes especially important when the adhesive bonding layer becomes thin, as is the case in evanescently coupled devices. These particles can be present already on the target wafer, necessitating thorough particle cleaning prior to  $\mu$ TP, as is the case with other die-to-wafer bonding approaches. A second source of particles is those that are introduced during the coupon pick-up. Again, this relates to the design of the tether structures: in general, one wants to use materials that allow for a clean break (SiN is a good candidate here), and at the same time, one wants to reduce the number of tethers per device as much as possible (fewer tethers breaking means a lower chance of particle formation). This, however, has to be traded-off with the yield of the release process. A second aspect that needs to be addressed is the performance of the transfer-printed devices. In particular, for semiconductor lasers and SOAs, improvements have to be made in the efficiency of the transfer-printed devices. This requires optimization in several aspects: (a) improvement of the III–V fabrication processes, which is realized by transferring the technology to a III–V foundry; (b) improvement of the optical coupling efficiency between the III–V coupon and Si or SiN waveguide circuit (e.g., by using passive taper structures using III–V regrowth); and (c) improvement of the heat dissipation of the transfer-printed devices. As for all evanescently coupled devices on a SiPh platform, the thermal impedance to the Si substrate is quite large due to the presence of a several-micron thick buried oxide layer (note that the few tens of nanometer thick adhesive bonding layer has a negligible impact on the thermal

resistance). This issue can be tackled either by incorporating thermal vias into the Si substrate, by mounting the III–V/Si PIC p-side down on a heat spreader, or by developing transfer-printable buried heterostructure lasers/SOAs. A third aspect that needs to be studied is the reliability of the transfer printed devices. The presence of the thin bonding layer could have an impact on reliability, e.g., when it comes to thermal cycling. All these aspects are part of running projects. Currently, we believe there are no show-stoppers that prevent this technology from maturing and yielding high-performance, reliable PICs. Next to maturing the technology, we will explore its capabilities further, toward the integration of sources in the visible and UV parts of the optical spectrum, the printing of single photon detectors and 2D materials, and the printing of non-SiPh wafers, such as thin-film LiNbO<sub>3</sub> or CMOS electronics wafers. We believe there is also a lot of value in developing  $\mu$ TP technology for device layer stacks that do not have a release layer, such as bulk CMOS electronics or other bulk materials.

In order for  $\mu$ TP technology to thrive, an eco-system needs to be set up of source wafer providers,  $\mu$ TP lines, and target wafer providers. This is work in progress on several EU-funded projects. Next to that, some standardization needs to happen, such that coupons from different vendors can be integrated on SiPh wafers from different vendors using different  $\mu$ TP pilot lines. This includes standardizing the optical interfaces between the SiPh and the coupons, standardizing the electrical interface (pads on the source and target for electrical interconnection and on-wafer testing), standardizing the coupon dimensions and array layout on the source wafer, standardizing process control monitoring (PCM) test structures, etc.

#### IV. CONCLUSIONS

Micro-transfer printing is a promising and versatile heterogeneous integration technology for the realization of advanced photonic systems-on-chip. Current demonstrations cover proof-of-concept integration of InP, GaAs, GaSb, LiNbO<sub>3</sub>, Si, and Ce:YIG devices on Si PICs. Several steps need to be taken to bring this technology to maturity, including setting up a supply chain, demonstrating the yield of the integration approach, and proving the reliability of the heterogeneously integrated devices.

#### ACKNOWLEDGMENTS

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#### AUTHOR DECLARATIONS

##### Conflict of Interest

The authors have no conflicts to disclose.

## Author Contributions

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## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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